High Speed Wallace Tree Multiplier

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Abstract – Achieving high speed integrated circuits with low power consumption is a major concern for the VLSI circuit designers. Most arithmetic operations are done using multiplier, which is the major power consuming element in the digital circuit. In the present scenario, Fast multipliers with less power consumption are leading with their performance, basically process of multiplication is realized in hardware in terms of shift and add operation. The optimization of adder has led to the improvement in performance of multiplier. In this paper, multiplier is proposed using modified full adder, carry save adder and carry select adder using binary to excess one converter, to bring out the best multiplier with low power and high speed. To analyze the efficiency of proposed design, the conventional Wallace tree multiplier structure is used. The designs are developed using Verilog HDL(vivado) and the functionalities are verified through simulation. Synthesis results of the multiplier shows an average reduction in power, delay compared to the existing approaches.

Index Terms – Wallace tree multiplier, fulladder, carry save adder, carry select adder and binary to excess one converter.

1. INTRODUCTION

The power consumption, delay and area are always been an important design considerations for any chip designer. Many DSP structures incorporate multipliers in their design. Delay of the circuit inevitably changes with the delay of the multiplier. Therefore research is going on to reduce the delay of multiplier so that the delay of whole circuit can be reduced. An early description of the Wallace tree multiplier was given by [1]. Wallace tree multiplier has been evolved as high speed and area efficient multiplier. The Wallace tree multiplier involves ANDing of multiplier and multiplicand bits for the generation of partial products. In second phase full adders and half adders has been used for the reduction of generated partial products in two rows.

Followed by addition of two rows using fast carry adders in the third stage. In recent years a lot of research work has been carried out to reduce the complexity of the multiplier. In [2], the reordering of partial products is employed in such a way so as to reduce the switching activity which leads to reduction in power. Partitioning the partial product tree into four groups and applying Dadda to one group and Wallace multiplier to another and so on also achieves power reduction [3].In [4], a full adder using 4:1 multiplexers is used in the reduction phase to reduce the power. In [5], full adder is designed using six 2:1 multiplexers. In [6] modified full adder is used in the reduction phase which produces less delay. In [7] multiplier is realized using carry save adder which reduces delay. In [8] multiplier is realized by carry select adder which consumes less power and less delay compared to above mentioned adders.

The rest of the paper is organized as follows: Section II discusses the related works of full adder. Section III presents the architecture of high speed adders. The discussion and results are summarized in section IV and finally section V, concludes the paper.

2. TRADITIONAL WALLACE TREE MULTIPLIER

Wallace proposed the column compression technique for fast multiplication operations in which the total delay is proportional to the logarithm of the word length of multiplier operand [1]. The Wallace tree multiplier with column compression technique is faster than array multipliers, because the delay in an array multiplier varies linearly, whereas in Wallace it varies logarithmically. Let us consider a N bits multiplication, N2 AND gates are required in order to generate the partial product terms and the number of reduction stages is given by S which is shown in (1)

$$S = \log_2 N \quad (1)$$

The number of half adders is at least N - 1, and is often much greater than N. Fig. 1 illustrates the reduction tree of 8 x 8 bits unsigned multiplier. Each dot represents a single-bit partial product. Starting from the right most column, when three bits come across, full adders and for two bits, half adders are used respectively. The sum and carry outputs for each adder at one stage are again represented as dots in the next stage and are used as inputs of adders in that stage (or sent directly to the final adder).

Each column has a certain order of magnitude of the partial products. The sum output at one stage reflect a dot in the same column at the next stage. The carry output at one stage reflects a dot in the column to its left i.e. one order of magnitude higher.

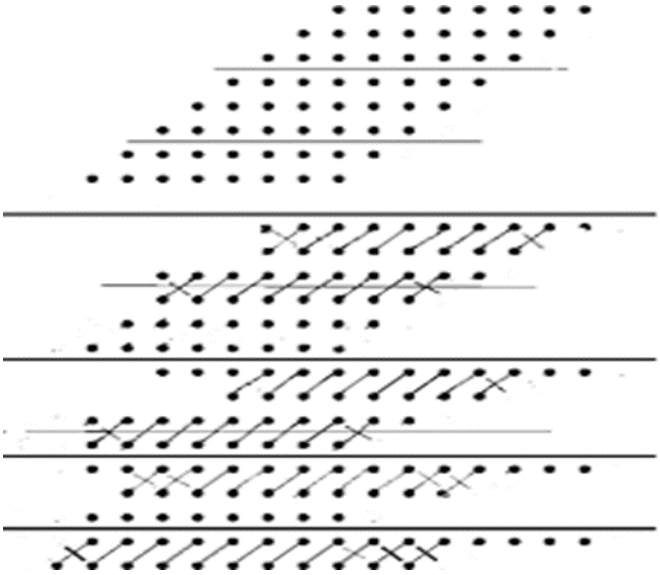

Figure 1: Wallace tree multiplier

In Wallace tree multiplier full adder is proposed in four different formats which is shown below figures.

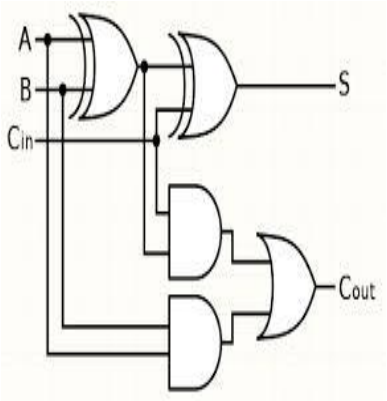

Figure2: conventional full adder

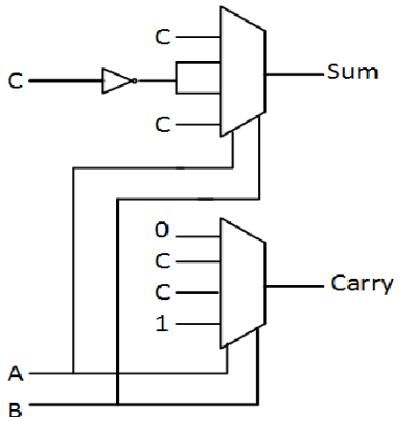

Figure3: full adder using 4:1 mux

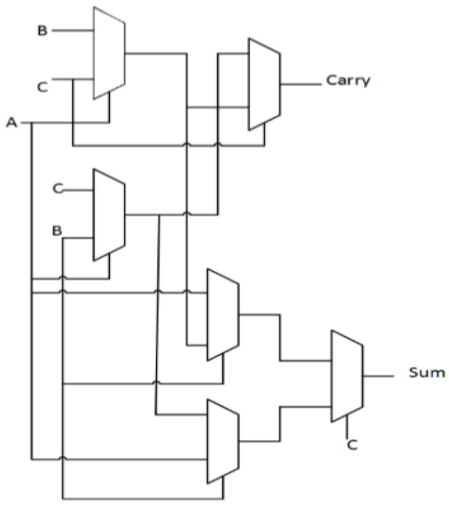

Figure 4: full adder using six 2:1 mux

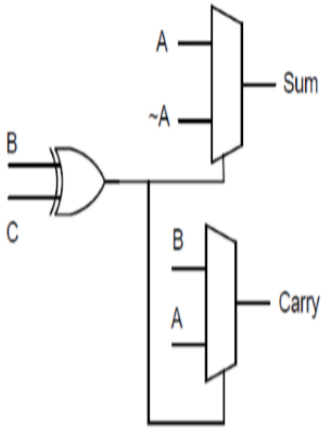

Figure 5:modified full adder

Table-1: Comparison of area, power and delay

Multiplier	Area(LUT'S)	Power(watts)	Delay(nS)
Conventional full adder	79	4.6	15.219
MUX Based full adder	81	4.707	15.599
Full adder using six 2:1 mux	81	4.677	14.899
Modified full adder	104	5.3	14.659

The above table shows the synthesis results of Wallace tree multiplier using different types of full adders. From the above table it is clear that multiplier being realized by modified full adder is the fastest circuit that has less propagation delay but it is consuming more power. In order to reduce the power we have implemented the multiplier using high speed adders which were discussed in section-III.

3. HIGH SPEED ADDERS

3.1 Carry save adder

Using carry save addition, the delay can be reduced further still. The idea is to take 3 numbers that we want to add together, x + y + z, and convert it into 2 numbers c + s such that x + y + z = c + s. Another way to look at it is that any carry over from one column gets put into the next column. Now, we can add together c and s, The important point is that c and s can be computed independently, and furthermore, each carry input (and sum input) can be computed independently from obtained partial products. This achieves our original goal of converting three numbers that we wish to add into two numbers that add up to the same sum, It is actually identical to the full adder, but with some of the signals renamed. Figure 6 shows a full adder and a carry save adder. A carry save adder simply is a full adder with the cin input renamed to z, the z output (the original "answer" output) renamed to s, and the cout output renamed to c.

x:			1	0	0	1	1
y:			1	1	0	0	1
z:	+		0	1	0	1	1
s:			0	0	0	0	1
c:	+	1	1	0	1	1	
sum:		1	1	0	1	1	1

Figure 6.1: carry save adder

```
x :   1 0 0 1 1
y :   1 1 0 0 1
z :   0 1 0 1 1
-----------------
s :   0 0 0 0 1
c : 1 1 0 1 1
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Figure 6.2: full adder

In the Wallace tree multiplier carry save adder logic goes this way, name all the partial product columns as A,B,C,…H and add according to block diagram.

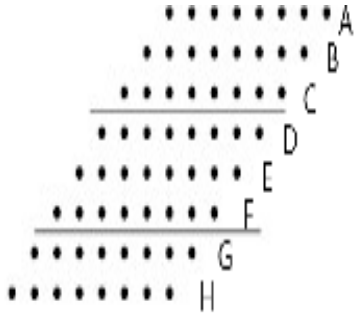

Figure 7: Block diagram of wallace multiplier using csa

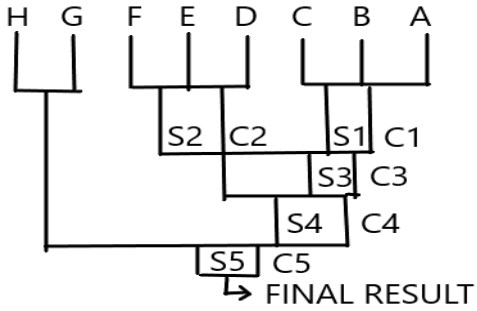

Figure 8: Carry save adder

Table-2: Comparison of Area, delay and delay

Multiplier	Area(LUT'S)	Power(watts)	Delay(nS)
Carry save adder	100	5.3	14.1

3.2 Carry select adder (BEC)

Wallace tree multiplier is designed with CSLA in order to increase the speed. This gives the solution for the problem of carry propagation delay by independently generating multiple carries and then selects a carry to obtain the sum. As we know CSLA is not area efficient as it uses multiple pairs of Ripple Carry Adders(RCA) partial sum and carry by considering cin=0 and cin =1,then final sum and carry are selected by multiplexers, this disadvantage made a reason to replace RCA in regular CSLA with binary to excess-1 converter(BEC).

BEC is replaced instead of RCA with cin = 1 in regular CSLA to achieve the lower area, power consumption and uses less number of logic gates, then final sum and carry is selected through MUX[9]. The importance of BEC logic stems from the large silicon area reduction when the CSLA with large number of bits are designed. In regular CLSA as the utilization of gates are more due to this power consumption also increases. Now by using BEC in regular CSLA we can reduce number of gates and simultaneously decreases power consumption [10]-[12].

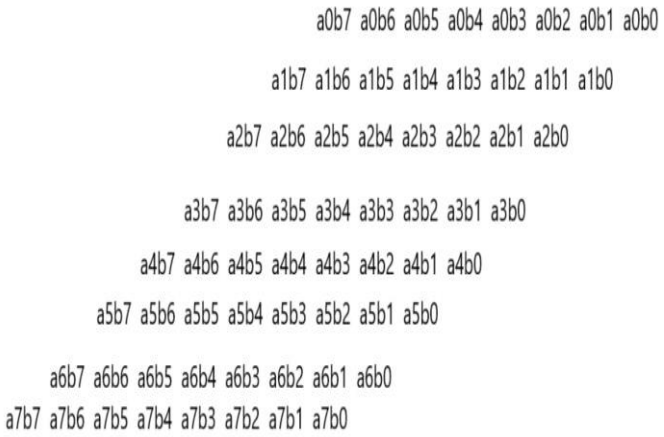

Figure9: Block diagram of Wallace partial products

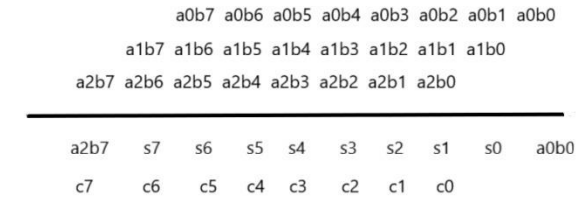

Figure10: First stage

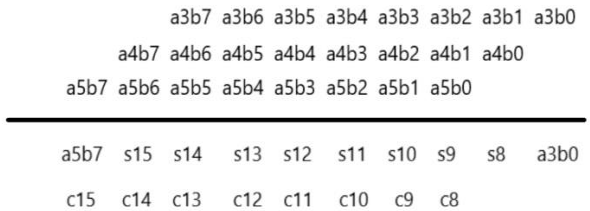

Figure11: second stage

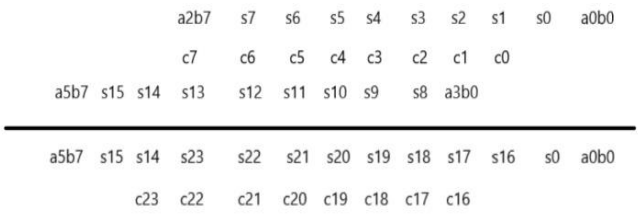

Figure12: Third stage

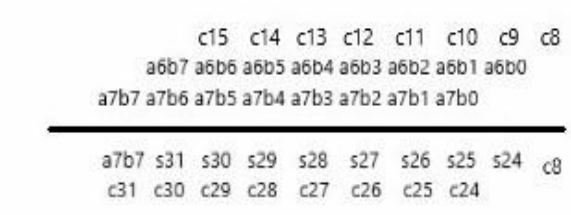

Figure13: fourth stage

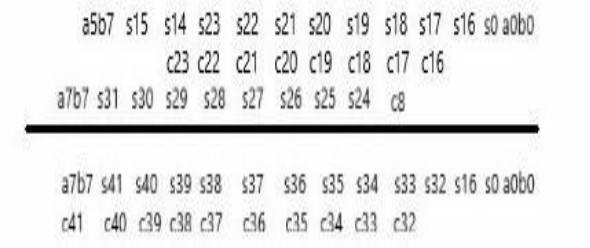

Figure14: Fifth stage

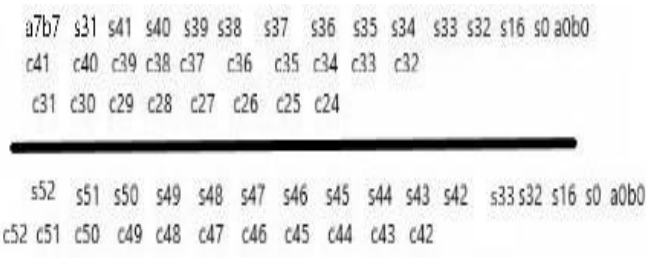

Figure15: sixth stage

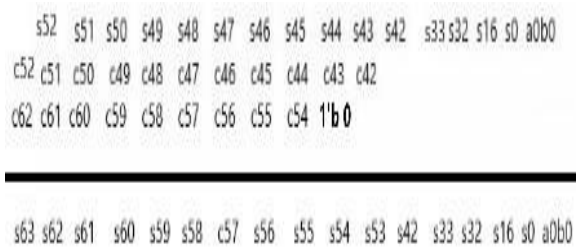

Figure16: Seventh stage

Results of sum [64-73] with c53=1 can be obtained by passing s[54-63] to binary to excess one convertor(BEC) as inputs. A sample of BEC is illustrated in Fig:17. Depending on the value of c53 either output of s[54-63] or output of s[64-73] will be chosen by multiplexer(MUX) as shown in Fig-18.

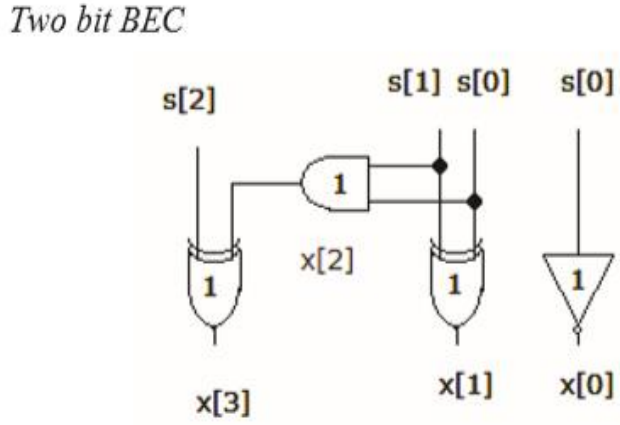

Figure17: BEC with partial products as inputs

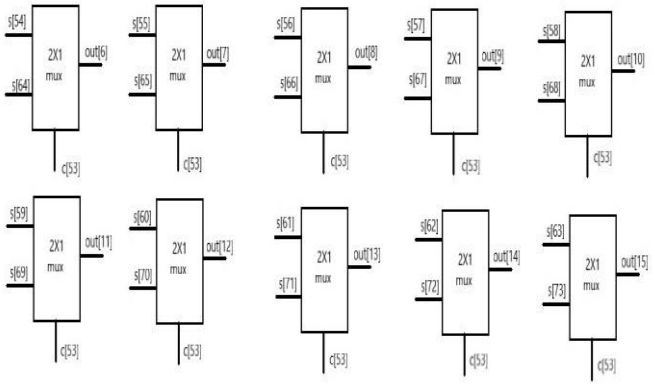

Figure18: multiplexers circuit

4. SYNTHESIS RESULTS

Table-3: Comparison of area, power and delay

Multiplier using	Area(LUT's)	Power(watts)	Delay(nsec)
Modified fulladder	104	5.3	14.6
Carry save adder	100	5.3	14.1
Carry select adder with BEC	100	3.8	12.6

The table shows the Synthesis results of Wallace Tree Multiplier using different adders. From the table it is clear that wallace tree multiplier when implemented using carry select adder there is reduction in power by 28.3% and delay got reduced by 13% compared to full adder and carry save adders.

Simulation results

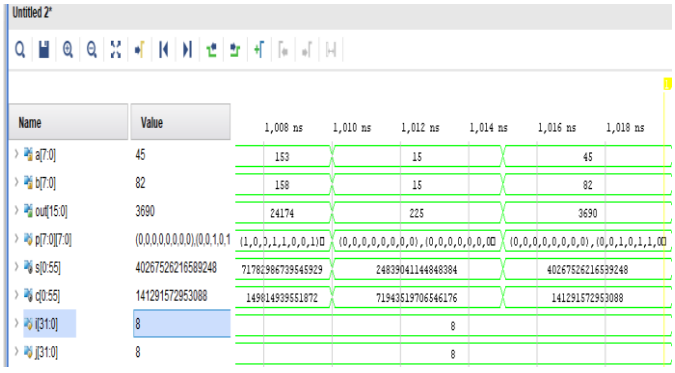

Figure19: Modified full adder simulation result

The Simulation results are carried out for wallace tree multiplier using various adders. The performance evaluation of Wallace Tree multiplier using modified full adder, carry save adder, carry select adder with BEC is carried out using Xilinx Vivado design suite 2017.4.

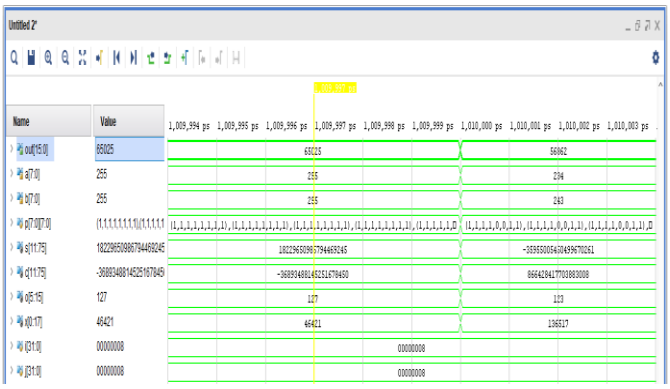

Figure20: Carry save adder simulation result

Figure21: Carry select adder with BEC

5. CONCLUSION

A Simple approach is proposed in this paper to reduce the power consumption of Wallace tree multiplier using CSLA. From the above results it is observed that the Wallace tree multiplier using CSLA with BEC is consuming less power, occupying less area when compared to Wallace tree multiplier using full adders and carry save adders.

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